

1. A process for forming a composite layer of low k silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate having closely spaced apart metal lines thereon, said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between closely spaced apart metal lines, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning characteristics, comprising the steps of:
- a) forming over said oxide layer and said metal lines a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between said closely spaced apart metal lines, until said low k silicon oxide dielectric material reaches the level of the top of said metal lines on said oxide layer; and
  - b) forming a second layer of low k silicon oxide dielectric material over said first layer at a higher deposition rate than said first layer.
2. The process of claim 1 wherein said steps to form said composite layer of low k silicon oxide dielectric material are all carried out in a single vacuum processing apparatus without removal of said semiconductor substrate from said vacuum apparatus.
3. The process of claim 2 wherein said second layer is deposited up to the desired overall thickness of the composite low k silicon oxide dielectric layer.
4. The process of claim 2 wherein said first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions is formed by reacting a carbon-substituted silane with a mild oxidant.
5. The process of claim 4 wherein said mild oxidant comprises hydrogen peroxide.
6. The process of claim 4 wherein said carbon-substituted silane is selected from the group consisting of monomethyl silane, dimethyl silane, and trimethyl silane.

7. The process of claim 4 wherein said carbon-substituted silane comprises a carbon-substituted silane having only primary hydrogens bonded to the carbon atoms and having the formula:  $\text{SiH}_x((\text{C})_y(\text{CH}_3)_z)_{(4-x)}$ , where x ranges from 1 to 3, y is an integer from 1 to 4 for a branched alkyl group and from 3 to 5 for a cyclic alkyl group, and z is  $2y+1$  for a branched alkyl group and  $2y-1$  for a cyclic alkyl group.

8. The process of claim 2 wherein said first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions is formed by reacting oxygen with either a carbon-substituted silane, a fluorine-substituted silane, or a mixture of same in a high density plasma.

9. The process of claim 2 wherein said second layer of low k silicon oxide dielectric material is formed over said first layer by reacting silane,  $\text{O}_2$ , and one or more reactants selected from the group consisting of  $\text{CH}_4$ ,  $\text{C}_4\text{F}_8$ , and  $\text{SiF}_4$  in a PECVD process, whereby said second layer of low k silicon oxide dielectric material is deposited at a higher deposition rate than said first layer.

10. A process for forming a composite layer of low k carbon-doped silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate, said composite layer of low k carbon-doped silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between closely spaced apart metal lines, deposition rates comparable to non carbon-doped silicon oxide, and without exhibiting via poisoning characteristics, comprising the steps of:

- a) forming over said oxide layer and said metal lines a first layer of low k carbon-doped silicon oxide dielectric material by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-doped silicon oxide dielectric material reaction product reaches the level of the top of said metal lines on the oxide layer to form a low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between said closely spaced apart metal lines; and
- b) forming a second layer of carbon-doped low k silicon oxide dielectric material over said first layer up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer by plasma enhanced chemical vapor deposition (PECVD), whereby said second layer of low k silicon oxide dielectric material is deposited at a higher deposition rate than said first layer.

11. The process of claim 10 wherein steps to form said composite layer of low k silicon oxide dielectric material are all carried out in a single vacuum processing apparatus without removal of said semiconductor substrate from said vacuum apparatus.

12. The process of claim 11 wherein said second layer of low k silicon oxide dielectric material is formed over said first layer in said PECVD process, by reacting silane, O<sub>2</sub>, and one or more reactants selected from the group consisting of CH<sub>4</sub>, C<sub>4</sub>F<sub>8</sub>, and SiF<sub>4</sub>.

13. The process of claim 1 wherein after said step of forming said first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between said closely spaced apart metal lines, said first layer is planarized prior to said step of forming said second layer of low k silicon oxide dielectric material.

14. The process of claim 13 wherein said step of planarizing said first layer of low k silicon oxide dielectric material further comprises a chemical mechanical polishing (CMP) step.

15. A composite layer of low k silicon oxide dielectric material on an oxide layer of an integrated circuit structure, said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning  
5 characteristics, comprising:

- a) a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposited until said low k silicon oxide dielectric material reaches the level of the top of metal lines on said oxide layer; and
- b) a second layer of low k silicon oxide dielectric material deposited over the first layer at a faster rate than the deposition rate of said first layer up to the desired overall thickness of the composite layer of low k carbon-doped silicon oxide dielectric material.

16. The composite layer of low k silicon oxide dielectric material of claim 15 wherein said first and second layers comprising said composite layer of low k silicon oxide dielectric material are all formed in a single vacuum processing apparatus without removal of said semiconductor substrate from said vacuum apparatus.

17. A composite layer of low k carbon-doped silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate, said composite layer of low k carbon-doped silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposition rates comparable to non carbon-doped silicon oxide, and without exhibiting via poisoning characteristics, comprising:

- a) a first layer of low k carbon-doped silicon oxide dielectric material formed by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-doped silicon oxide dielectric material reaction product reaches the level of the top of metal lines on the oxide layer; and
- b) a second layer of carbon-doped low k silicon oxide dielectric material formed over said first layer by plasma enhanced chemical vapor deposition (PECVD) up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer.